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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,453	12/09/2003	Rajeev Joshi	11948.25	4432

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EXAMINER	
ZARNEKE, DAVID A	
ART UNIT	**PAPER NUMBER**
2891	

DATE MAILED: 08/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,453	JOSHI ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *20-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/06 by es/06 by
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Group I, claims 1-19 in the reply filed on 7/11/05 is acknowledged. The traversal is on the ground(s) that the restriction requirement doesn't assert that the species are independent. Also, the reason for restriction is challenged because the alternative process is included in the comprising language of the claims.

This is not found persuasive because the restriction requirement does assert the independence of the claims statement in the restriction that the inventions "have acquired a separate status in the art as shown by their different classification" is the assertion of independence. This meets the requirements of MPEP802 and 802.1. Further, the fact that the claims have comprising language is would not encompass the alternative process recited because the claims specifically state that the chip is attached to the substrate using the conductive adhesive.

The requirement is still deemed proper and is therefore made FINAL.

Rejections over Lau, Flip Chip Technologies, McGraw-Hill, 1996, pp. 301-314

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Lau, Flip Chip Technologies, McGraw-Hill, 1996, pp. 301-314.

Lau (figure 9.17, page 314) teaches a wafer-level chip scale package, comprising: a chip containing a stud bump (box below figure states "bump size", therefore chip has bump thereon); a conductive substrate (PCB with electrodes [the boxes on the PCB] thereon); and an adhesive material containing conductive particles located between the chip and the substrate.

Regarding claim 2, Lau teaches the conductive particles are located between the stud bump and the substrate.

With respect to claim 3, Lau (page 313) teaches the conductive particles comprise metal with an insulating layer.

As to claim 4, Lau (page 301) teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

In re claim 5, Lau teaches the chip contains an integrated circuit in communication with a chip pad (the bump is attached to the pad of the chip which in turn electrically connects to the integrated circuit).

Claims 11 and 12 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Lau, Flip Chip Technologies, McGraw-Hill, 1996, pp. 301-314.

Lau (figure 9.17, page 314) teaches a wafer-level chip scale package, comprising: a chip containing a stud bump (box below figure states "bump size", therefore chip has bump thereon); a conductive substrate (PCB with electrodes [the boxes on the PCB] thereon); and an adhesive

material containing conductive particles located between the chip and the substrate with at least one conductive particle located between the stud bump and the bond pad.

Regarding claim 12, Lau (page 301) teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

Claim 19 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Lau, Flip Chip Technologies, McGraw-Hill, 1996, pp. 301-314.

Lau teaches an electronic apparatus containing a packaged semiconductor device, the device comprising: a chip containing a stud bump (box below figure states "bump size", therefore chip has bump thereon); a conductive substrate (PCB with electrodes [the boxes on the PCB] thereon); and an adhesive material containing conductive particles located between the chip and the substrate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lau, Flip Chip Technologies, McGraw-Hill, 1996, pp. 301-314, as applied to claim 1 above.

Regarding claim 6, Lau fails to specifically teach the conductive substrate has been patterned. But it would have been obvious to one of ordinary skill in the art at the time of the invention to use a patterned conductive substrate because one is implied since the pad must connect to a patterned conductive line on the surface of the chip. Further, figure 9.4 on page 305 shows the connecting areas (chip pads) as being at the junction of electrodes.

Regarding claim 7, while Lau fails to teach the patterned conductive substrate serves as a redistribution layer, it would have been obvious to one of ordinary skill in the art to use the conductive substrate as a redistribution layer because a redistribution layer is conventionally known in the art to used in electrically connecting pads and/or bumps of a different configuration than the substrate to which they are attached. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

With respect to claims 8 and 9, while Lau fails to teach the conductive substrate comprises copper or a copper foil, it would have been obvious to one of ordinary skill in the art at the time of the invention to use copper or a copper foil as the conductive substrate because they are conventionally known in the art materials used as conductive substrates. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

As to claim 10, while Lau fails to teach the stud bump comprises Cu, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Cu as the stud bump because Cu is a conventionally known in the art material used as a stud bump. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lau, Flip Chip Technologies, McGraw-Hill, 1996, pp. 301-314, as applied to claim 11 above.

Regarding claim 13, while Lau fails to teach the patterned conductive substrate serves as a redistribution layer, it would have been obvious to one of ordinary skill in the art to use the conductive substrate as a redistribution layer because a redistribution layer is conventionally known in the art to used in electrically connecting pads and/or bumps of a different configuration than the substrate to which they are attached. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

With respect to claim 14, while Lau fails to teach the conductive substrate comprises a copper foil, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a copper foil as the conductive substrate because they are conventionally known

in the art materials used as conductive substrates. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lau, Flip Chip Technologies, McGraw-Hill, 1996, pp. 301-314.

Lau (figure 9.17, page 314) teaches a packaged semiconductor device, comprising: a chip containing a stud bump (box below figure states "bump size", therefore chip has bump thereon); a patterned conductive substrate (PCB with electrodes [the boxes on the PCB] thereon); and an adhesive material containing conductive particles located between the chip and the substrate with at least one conductive particle located between the stud bump and the bond pad.

Lau fails to specifically teach the conductive substrate has been patterned. But it would have been obvious to one of ordinary skill in the art at the time of the invention to use a patterned conductive substrate because one is implied since the pad must connect to a patterned conductive line on the surface of the chip.

Regarding claim 16, Lau (page 301) teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste.

With respect to claim 17, while Lau fails to teach the conductive substrate comprises a copper foil, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a copper foil as the conductive substrate because they are conventionally known in the art materials used as conductive substrates. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

As to claim 18, while Lau fails to teach the patterned conductive substrate serves as a redistribution layer, it would have been obvious to one of ordinary skill in the art to use the

conductive substrate as a redistribution layer because a redistribution layer is conventionally known in the art to used in electrically connecting pads and/or bumps of a different configuration than the substrate to which they are attached. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

Rejections over Otsuka, US Patent 5,949,142

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Otsuka, US Patent 5,949,142.

Otsuka (figure 3) teaches a wafer-level chip scale package, comprising: a chip [2] containing a stud bump [2a]; a conductive substrate [5]; and an adhesive material [6] containing conductive particles [6a] located between the chip and the substrate.

Regarding claim 2, Otsuka teaches a conductive particle is located between the stud bump and the substrate (figure 3).

With respect to claim 3, Otsuka teaches the conductive particles comprise metal with an insulating layer (4, 13+).

As to claim 4, Otsuka teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (4, 65+).

In re claim 5, Otsuka teaches the chip contains an integrated circuit in communication with a chip pad (4, 65+).

Regarding claim 6 Otsuka teaches the conductive substrate has been patterned (5, 4+).

With respect to claim 7, Otsuka teaches the patterned conductive substrate serves as a redistribution layer (Figure 3; the metal pattern [4a] redistributes the electrical path from the chip pad to the interlevel conductive bump [4c]).

Claims 11-13 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Otsuka, US Patent 5,949,142.

Otsuka (figure 3) teaches a wafer-level chip scale package, comprising: a chip [2] containing a stud bump [2a]; a conductive substrate [5]; and an adhesive material [6] containing conductive particles located between the chip and the substrate with at least one conductive particle [6a] located between the stud bump and the bond pad.

As to claim 12, Otsuka teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (4, 65+).

With respect to claim 13, Otsuka teaches the patterned conductive substrate serves as a redistribution layer (Figure 3; the metal pattern [4a] redistributes the electrical path from the chip pad to the interlevel conductive bump [4c]).

Claims 15, 16 and 18 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Otsuka, US Patent 5,949,142.

Otsuka (figure 3) teaches a packaged semiconductor device, comprising: a chip [2] containing a stud bump [2a]; a patterned conductive substrate [5]; and an adhesive material [6]

containing conductive particles [6a] located between the chip and the substrate with at least one conductive particle located between the stud bump and the bond pad.

As to claim 16, Otsuka teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (4, 65+).

With respect to claim 18, Otsuka teaches the patterned conductive substrate serves as a redistribution layer (Figure 3; the metal pattern [4a] redistributes the electrical path from the chip pad to the interlevel conductive bump [4c]).

Claim 19 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Otsuka, US Patent 5,949,142.

Otsuka (figure 3) teaches an electronic apparatus containing a packaged semiconductor device, the device comprising: a chip [2] containing a stud bump [2a]; a conductive substrate [5]; and an adhesive material [6] containing conductive particles [6a] located between the chip and the substrate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otsuka, US Patent 5,949,142, as applied to claim 1 above..

Regarding claims 8 and 9, while Otsuka fails to teach the conductive substrate comprises copper or a copper foil, it would have been obvious to one of ordinary skill in the art at the time of the invention to use copper or a copper foil as the conductive substrate because they are conventionally known in the art materials used as conductive substrates. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07)..

As to claim 10, while Otsuka, which teaches the use of silver as the stud bump, fails to teach the stud bump comprises Cu, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Cu as the stud bump because Cu is a conventionally known

equivalent art used in the art as a stud bump. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Otsuka, US Patent 5,949,142, as applied to claim 11 above.

While Otsuka fails to teach the conductive substrate comprises a copper foil, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a copper foil as the conductive substrate because they are conventionally known in the art materials used as conductive substrates. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Otsuka, US Patent 5,949,142, as applied to claim 15 above.

While Otsuka fails to teach the conductive substrate comprises a copper foil, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a copper foil as the conductive substrate because they are conventionally known in the art materials used as conductive substrates. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-Th 7:30 AM-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David A. Zarneke
Primary Examiner
July 29, 2005